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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2181	11

DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/787,218	ISHIDA ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 Mar 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 14-22* is/are rejected.

7)☒ Claim(s) *9 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *10 May 2001* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,7,10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

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DETAILED ACTION

Drawings

1. The corrected drawings were received on 10 May 2001. These drawings are acceptable.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Number 95 on Page 19 Line 8. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Number 110 in Figure 8. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because Step S4 of Figure 15 includes the term "UADLET". The Examiner recommends changing "UADLET" to "QUADLET" and will

assume said change for the purposes of examination. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claim 9 is objected to because of the following informalities: Line 8 of Claim 9 (Page 50 Line 27) is duplicated as Line 9 of Claim 9 (Page 51 Line 1). Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 1, 2, 9, 14, 16, 17, 19, 20, and 22 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chou et al. ("Chou").

In reference to Claim 1, Chou teaches a 1394 link for sending and receiving data packets on a bus connected to other nodes (See Figure 2 and Column 6 Lines 49-60); a means for writing received packet data into a main memory that is inherently randomly accessible (analogous to the randomly accessible packet storage means of Claim 1) (See Figure 2 and Column 3 Lines 47-52); and a packet division means that writes the packet header (analogous to the control information of Claim 1) to a special area of the memory, writes the protocol header (analogous to the first data of the packet for a first layer of Claim 1) to a first data area of the memory, writes the content data (analogous to the second data of the packet for a second layer, which is a layer above the first layer, of Claim 1) to a second area of memory, stores the protocol headers in adjacent memory locations, and stores the content data in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6).

In reference to Claim 2, Chou teaches the limitations as applied to Claim 1 above, and further teaches a protocol header (analogous to the command header of

Claim 2) and content data (analogous to data used by an application layer of Claim 2) (See Column 2 Lines 40-45).

In reference to Claim 14, Chou teaches the limitations as applied to Claim 1 above, and further teaches that the data transfer of the device is in accordance with the IEEE 1394 standard (See Figure 2, Column 2 Lines 63-67, and Column 3 Lines 1-7).

In reference to Claim 17, Chou teaches the limitations as applied to Claim 1 above, and further teaches that the device is included as part of electronic equipment (See Figure 2 and Column 6 Lines 30-32) which further includes a CPU for processing the data received through the data transfer control device (See Figure 2, Column 6 Lines 66-67, and Column 7 Lines 1-2), a mass storage device for storing the data that has been subjected to processing (See Figure 2 and Column 6 Lines 61-64), and a display for outputting the data that has been subjected to processing (See Figure 2, Column 7 Lines 3-17).

In reference to Claim 20, Chou teaches the limitations as applied to Claim 1 above, and further teaches that the CPU can take in data to be subject to processing (See Figure 2). Since the internal bus is bidirectional (See Figure 2 and Column 6 Lines 47-48), and since the interface circuitry can both send and receive data (See Figure 2 and Column 6 Lines 49-60), it is inherent that the CPU can perform processing on data that is to be transferred to another node through the interface circuit and the bus. Chou further teaches that data to be subjected to processing can be taken in through a keyboard, a mouse, or the 1394 link (See Figure 2 and Column 7 Lines 3-10).

In reference to Claim 9, Chou teaches a 1394 link for sending and receiving data packets on a bus connected to other nodes (See Figure 2 and Column 6 Lines 49-60); a main memory which is inherently randomly accessible (analogous to the randomly accessible packet storage means of Claim 9) (See Figure 2 and Column 3 Lines 47-52); a means for writing packet data received from the link to the randomly accessible main memory (See Figure 2 and Column 3 Lines 47-52); and the division of the packet storage means into an area for the packet header (analogous to the control information of Claim 9) and an area for the packet data, said area for packet data divided into an area for storing the protocol header (analogous to the first data area for storing first data of the packet for a first layer, of Claim 9) and an area for the content data (analogous to a second data area for storing the second data of the packet for a second layer, which is a layer above the first layer, of Claim 9). Chou further teaches that the protocol headers are stored in adjacent memory locations and the content data is stored in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6). Chou further teaches that the interface circuit can both send and receive communications through the 1394 link, so it would inherently be able to read the data in the main memory and send it to the link (See Figure 2 and Column 6 Lines 49-60).

In reference to Claim 16, Chou teaches the limitations as in Claim 9 above, and further teaches that the data transfer of the device is in accordance with the IEEE 1394 standard (See Figure 2, Column 2 Lines 63-67, and Column 3 Lines 1-7).

In reference to Claim 19, Chou teaches the limitations as in Claim 9 above, and further teaches that the device is included as part of electronic equipment (See Figure 2 and Column 6 Lines 30-32) which further includes a CPU for processing the data received through the data transfer control device (See Figure 2, Column 6 Lines 66-67, and Column 7 Lines 1-2), a mass storage device for storing the data that has been subjected to processing (See Figure 2 and Column 6 Lines 61-64), and a display for outputting the data that has been subjected to processing (See Figure 2, Column 7 Lines 3-17).

In reference to Claim 22, Chou teaches the limitations as applied to Claim 9 above, and further teaches that the CPU can take in data to be subject to processing (See Figure 2). Since the internal bus is bidirectional (See Figure 2 and Column 6 Lines 47-48), and since the interface circuitry can both send and receive data (See Figure 2 and Column 6 Lines 49-60), it is inherent that the CPU can perform processing on data that is to be transferred to another node through the interface circuit and the bus. Chou further teaches that data to be subjected to processing can be taken in through a keyboard, a mouse, or the 1394 link (See Figure 2 and Column 7 Lines 3-10).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 2, 9, 14, 16, 17, 19, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haneda et al. ("Haneda") in view of Chou.

In reference to Claim 1, Haneda teaches a data transfer control device for transferring data between a plurality of nodes connected to a bus comprising link means which provide services for packet transfer between nodes (See Abstract and Figure 5 of Haneda) and write means which writes a packet that has been received through the link means to a packet storage means that is inherently randomly accessible (See Abstract and Figure 5 of Haneda). Haneda does not teach a packet division means which writes control information of the packet to a control information area of the packet storage means, writes first data of the packet for a first layer to a first data area of the packet storage means, and writes second data of the packet for a second layer that is a layer above the first layer to a second data area of the packet storage means. Chou teaches a packet division means that writes the packet header (analogous to the control information of Claim 1) to a special area of the memory, writes the protocol header (analogous to the first data of the packet for a first layer) to a first data area of the memory, writes the content data (analogous to the second data of the packet for a second layer, which is a layer above the first layer, of Claim 1) to a second area of memory, stores the protocol headers in adjacent memory locations, and stores the content data in adjacent memory locations (See Figure 3, Column 2 Lines 63-67,

Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou).

In reference to Claim 2, Haneda teaches the limitations as applied to Claim 1 above. Haneda does not teach a packet division means which writes control information of the packet to a control information area of the packet storage means, writes first data of the packet for a first layer to a first data area of the packet storage means, and writes second data of the packet for a second layer that is a layer above the first layer to a second data area of the packet storage means; and that the first data is command data used by the protocol of the first layer and the second data is data used by an application layer. Chou teaches a packet division means that writes the packet header (analogous to the control information of Claim 2) to a special area of the memory, writes the protocol header (analogous to the first data of the packet for a first layer, of Claim 2) to a first data area of the memory, writes the content data (analogous to the second data of the packet for a second layer, which is a layer above the first layer, of Claim 2) to a second area of memory, stores the protocol headers in adjacent memory locations, and stores the content data in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou); and a protocol header (analogous to the command header of Claim 2) and content data (analogous to data used by an application layer of Claim 2) (See Column 2 Lines 40-45 of Chou).

In reference to Claim 14, Haneda teaches the limitations as applied to Claim 1 above. Haneda does not teach a packet division means which writes control

information of the packet to a control information area of the packet storage means, writes first data of the packet for a first layer to a first data area of the packet storage means, and writes second data of the packet for a second layer that is a layer above the first layer to a second data area of the packet storage means; and that the first data is command data used by the protocol of the first layer and the second data is data used by an application layer and that the data transfer of the device is in accordance with the IEEE 1394 standard. Chou teaches packet division means that writes the packet header (analogous to the control information of Claim 14) to a special area of the memory, writes the protocol header (analogous to the first data of the packet for a first layer, of Claim 14) to a first data area of the memory, writes the content data (analogous to the second data of the packet for a second layer, which is a layer above the first layer, of Claim 14) to a second area of memory, stores the protocol headers in adjacent memory locations, and stores the content data in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou); and that the data transfer of a device is in accordance with the IEEE 1394 standard (See Figure 2, Column 2 Lines 63-67, and Column 3 Lines 1-7 of Chou).

In reference to Claim 17, Haneda teaches the limitations as applied to Claim 1 above. Haneda does not teach a packet division means which writes control information of the packet to a control information area of the packet storage means, writes first data of the packet for a first layer to a first data area of the packet storage means, and writes second data of the packet for a second layer that is a layer above the

first layer to a second data area of the packet storage means; and a device which performs given processing on data that has been received from another node through the data transfer control device and a bus, and a device which outputs or stores data that has been subjected to processing. Chou teaches packet division means that writes the packet header (analogous to the control information of Claim 17) to a special area of the memory, writes the protocol header (analogous to the first data of the packet for a first layer, of Claim 17) to a first data area of the memory, writes the content data (analogous to the second data of the packet for a second layer, which is a layer above the first layer, of Claim 17) to a second area of memory, stores the protocol headers in adjacent memory locations, and stores the content data in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou); and that the device further includes a CPU for processing the data received through the data transfer control device (See Figure 2, Column 6 Lines 66-67, and Column 7 Lines 1-2 of Chou), a mass storage device for storing the data that has been subjected to processing (See Figure 2 and Column 6 Lines 61-64 of Chou), and a display for outputting the data that has been subjected to processing (See Figure 2, Column 7 Lines 3-17 of Chou).

In reference to Claim 20, Haneda teaches the limitations as applied to Claim 1 above. Haneda does not teach packet division means which writes control information of the packet to a control information area of the packet storage means, writes first data of the packet for a first layer to a first data area of the packet storage means, and writes second data of the packet for a second layer that is a layer above the first layer to a

second data area of the packet storage means; a device which performs given processing on data that is to be transferred to another node through the data transfer control device and a bus, and a device which takes in data to be subjected to processing. Chou teaches packet division means that writes the packet header (analogous to the control information of Claim 20) to a special area of the memory, writes the protocol header (analogous to the first data of the packet for a first layer, of Claim 20) to a first data area of the memory, writes the content data (analogous to the second data of the packet for a second layer, which is a layer above the first layer, of Claim 20) to a second area of memory, stores the protocol headers in adjacent memory locations, and stores the content data in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou); and that the CPU can take in data to be subject to processing (See Figure 2 of Chou). Since the internal bus is bidirectional (See Figure 2 and Column 6 Lines 47-48 of Chou), and since the interface circuitry can both send and receive data (See Figure 2 and Column 6 Lines 49-60 of Chou), it is inherent that the CPU can perform processing on data that is to be transferred to another node through the interface circuit and the bus. Chou further teaches that data to be subjected to processing can be taken in through a keyboard, a mouse, or the 1394 link (See Figure 2 and Column 7 Lines 3-10 of Chou).

In reference to Claim 9, Haneda teaches a data transfer control device for transferring data between a plurality of nodes connected to a bus comprising link means which provide services for packet transfer between nodes (See Abstract and Figures 5

and 6 of Haneda), packet storage means for storing a packet that is inherently randomly accessible (See Abstract and Figures 5 and 6 of Haneda), and write means which writes a packet that has been received from another node through the link means to a packet storage means (See Abstract and Figures 5 and 6 of Haneda). Haneda does not teach a means which reads the packet that has been written to the packet storage means and transfers the packet to the link means and a division of the packet storage means into an area for the control information and an area for the packet data, said area for packet data divided into a first data area for storing first data of the packet for a first layer and a second data area for storing the second data of the packet for a second layer. Chou teaches a division of the packet storage means into an area for the packet header (analogous to the control information of Claim 9) and an area for the packet data, said area for packet data divided into an area for storing the protocol header (analogous to the first data area for storing first data of the packet for a first layer of Claim 9) and an area for the content data (analogous to a second data area for storing the second data of the packet for a second layer, which is a layer above the first layer, of Claim 9). Chou further teaches that the protocol headers are stored in adjacent memory locations and the content data is stored in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6). Chou further teaches that the interface circuit can both send and receive communications through the 1394 link, so it would inherently be able to read the data in the main memory and send it to the link (See Figure 2 and Column 6 Lines 49-60).

In reference to Claim 16, Haneda teaches the limitations as applied to Claim 9 above. Haneda does not teach a means which reads the packet that has been written to the packet storage means and transfers the packet to the link means and a division of the packet storage means into an area for the control information and an area for the packet data, said area for packet data divided into a first data area for storing first data of the packet for a first layer and a second data area for storing the second data of the packet for a second layer; and that the data transfer of the device is in accordance with the IEEE 1394 standard. Chou teaches a division of the packet storage means into an area for the packet header (analogous to the control information of Claim 16) and an area for the packet data, said area for packet data divided into an area for storing the protocol header (analogous to the first data area for storing first data of the packet for a first layer of Claim 16) and an area for the content data (analogous to a second data area for storing the second data of the packet for a second layer, which is a layer above the first layer, of Claim 16). Chou further teaches that the protocol headers are stored in adjacent memory locations and the content data is stored in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou). Chou further teaches that the interface circuit can both send and receive communications through the 1394 link, so it would inherently be able to read the data in the main memory and send it to the link (See Figure 2 and Column 6 Lines 49-60 of Chou). Chou further teaches that the data transfer of a device is in accordance with the IEEE 1394 standard (See Figure 2, Column 2 Lines 63-67, and Column 3 Lines 1-7 of Chou).

In reference to Claim 19, Haneda teaches the limitations as applied to Claim 9 above. Haneda does not teach a means which reads the packet that has been written to the packet storage means and transfers the packet to the link means and a division of the packet storage means into an area for the control information and an area for the packet data, said area for packet data divided into a first data area for storing first data of the packet for a first layer and a second data area for storing the second data of the packet for a second layer; a device which performs given processing on data that has been received from another node through the data transfer control device and a bus, and a device which outputs or stores data that has been subjected to processing. Chou teaches a division of the packet storage means into an area for the packet header (analogous to the control information of Claim 19) and an area for the packet data, said area for packet data divided into an area for storing the protocol header (analogous to the first data area for storing first data of the packet for a first layer of Claim 19) and an area for the content data (analogous to a second data area for storing the second data of the packet for a second layer, which is a layer above the first layer, of Claim 19). Chou further teaches that the protocol headers are stored in adjacent memory locations and the content data is stored in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3 Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou). Chou further teaches that the interface circuit can both send and receive communications through the 1394 link, so it would inherently be able to read the data in the main memory and send it to the link (See Figure 2 and Column 6 Lines 49-60 of Chou). Chou further teaches that the device further includes a CPU for

processing the data received through the data transfer control device (See Figure 2, Column 6 Lines 66-67, and Column 7 Lines 1-2 of Chou), a mass storage device for storing the data that has been subjected to processing (See Figure 2 and Column 6 Lines 61-64 of Chou), and a display for outputting the data that has been subjected to processing (See Figure 2, Column 7 Lines 3-17 of Chou).

In reference to Claim 22, Haneda teaches the limitations as applied to Claim 9 above. Haneda does not teach a means which reads the packet that has been written to the packet storage means and transfers the packet to the link means and a division of the packet storage means into an area for the control information and an area for the packet data, said area for packet data divided into a first data area for storing first data of the packet for a first layer and a second data area for storing the second data of the packet for a second layer; a device which performs given processing on data that is to be transferred to another node through the data transfer control device and a bus, and a device which takes in data to be subjected to processing. Chou teaches a division of the packet storage means into an area for the packet header (analogous to the control information of Claim 22) and an area for the packet data, said area for packet data divided into an area for storing the protocol header (analogous to the first data area for storing first data of the packet for a first layer of Claim 22) and an area for the content data (analogous to a second data area for storing the second data of the packet for a second layer, which is a layer above the first layer, of Claim 22). Chou further teaches that the protocol headers are stored in adjacent memory locations and the content data is stored in adjacent memory locations (See Figure 3, Column 2 Lines 63-67, Column 3

Lines 1-7, Column 3 Lines 64-67, Column 4, Column 5, and Column 6 Lines 1-6 of Chou). Chou further teaches that the interface circuit can both send and receive communications through the 1394 link, so it would inherently be able to read the data in the main memory and send it to the link (See Figure 2 and Column 6 Lines 49-60 of Chou). Chou further teaches that the CPU can take in data to be subject to processing (See Figure 2 of Chou). Since the internal bus is bidirectional (See Figure 2 and Column 6 Lines 47-48 of Chou), and since the interface circuitry can both send and receive data (See Figure 2 and Column 6 Lines 49-60 of Chou), it is inherent that the CPU can perform processing on data that is to be transferred to another node through the interface circuit and the bus. Chou further teaches that data to be subjected to processing can be taken in through a keyboard, a mouse, or the 1394 link (See Figure 2 and Column 7 Lines 3-10 of Chou).

One of ordinary skill in the art at the time the invention was made would combine the device of Haneda with the device of Chou, resulting in the inventions of Claims 1, 2, 9, 14, 16, 17, 19, 20, and 22, in order to prevent errors from occurring when the data field may contain a header and content, as when the CIP Transport Protocol is used, and wherein some data fields may only contain the header and no other content (See Column 2 Lines 29-60 of Chou).

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou as applied to Claim 1 above, and further in view of Nakamura et al. ("Nakamura").

In reference to Claim 3, Chou teaches the limitations as applied to Claim 1 above. Chou does not teach the data transfer machine further comprising area management means which makes a full signal go active when the second data area is full, to inhibit the write means from writing the second data to the second data area, and makes and empty signal go active when the second data area is empty, to inhibit the second layer from reading the second data from the second data area. Nakamura teaches a device that counts packets read from and written to a memory, and inhibits reading transmission data from the memory when the memory is empty and inhibits writing reception data to the memory when the memory is full (See Abstract of Nakamura).

One of ordinary skill in the art at the time the invention was made would combine the device of Chou with the device of Nakamura, resulting in the invention of Claim 3, in order to accurately implement packet data reads and writes to and from memory (See Abstract of Nakamura).

12. Claims 4, 5, 6, 8, 15, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou as applied to Claim 1 above, and further in view of Gehman and Kobayashi.

In reference to Claim 4, Chou teaches the limitations as applied to Claim 1 above. Chou does not teach a request packet which is used for starting a transaction being transmitted to a responding node, transaction identification information comprised within the request packet including indication information which indicates processing to

be performed when a response packet from the responding node is received, and the control information and the first and second data of the response packet being written into an area specified by the indication information within the transaction identification information of the response packet when the response packet from the responding node is received. Gehman teaches that data can be obtained from a node by sending a read request packet, according to the IEEE 1394 Standard, which contains a tcode field. The node then responds by packetizing the data according to the 1394 Standard and sends it to the requesting node. The response packet contains information regarding the destination address for the data at the destination node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the tcode field of a 1394 Standard packet can provide information about the process to be executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). The packet of Chou is analogous to the request and response packets of Claim 4 and functions in an analogous matter.

In reference to Claim 5, Chou teaches a means which performs the processing indicated by the identification information of the response packet when the response packet of the responding node is received (See Figure 2, Column 6 Lines 43-48, and Column 7 Lines 3-10 of Chou). Chou does not teach a means which makes transaction identification information within a request packet include indication information which indicates processing to be performed after reception of a response packet from a responding node when the request packet which is used for starting a transaction is transmitted to the responding node. Gehman teaches that data can be obtained from a node by sending a read request packet, according to the IEEE 1394 Standard, which

contains a tcode field. The node then responds by packetizing the data according to the 1394 Standard and sends it to the requesting node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the tcode field of a 1394 Standard packet can provide information about the process to be executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). The packet of Chou is analogous to the request and response packets of Claim 5 and functions in an analogous matter.

In reference to Claim 6, Chou teaches the limitations as applied to Claim 5 above. Chou does not teach a means which makes transaction identification information within a request packet include indication information which indicates processing to be performed after reception of a response packet from a responding node when the request packet which is used for starting a transaction is transmitted to the responding node, and wherein control information and data of the response packet are written into an area specified by the indication information within the transaction identification information of the response packet when the response packet from the responding node is received. Gehman teaches that data can be obtained from a node by sending a read request packet, according to the IEEE 1394 Standard, which contains a tcode field. The node then responds by packetizing the data according to the 1394 Standard and sends it to the requesting node. The response packet contains information regarding the destination address for the data at the destination node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the tcode field of a 1394 Standard packet can provide information about the process to be executed (See Figure

7 and Column 5 Lines 35-42 of Kobayashi). The packet of Chou is analogous to the request and response packets of Claim 6 and functions in an analogous matter.

In reference to Claim 7, Chou teaches the limitations as applied to Claim 5 above. Chou does not teach a means which makes transaction identification information within a request packet include indication information which indicates processing to be performed after reception of a response packet from a responding node when the request packet which is used for starting a transaction is transmitted to the responding node, and a given bit of the transaction identification information being previously reserved as a bit for expressing the indication information. Gehman teaches that data can be obtained from a node by sending a read request packet, according to the IEEE 1394 Standard, which contains a tcode field. The node then responds by packetizing the data according to the 1394 Standard and sends it to the requesting node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the tcode field of a 1394 Standard packet can provide information about the process to be executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). Since the tcode field conveys different types of information, such as packet format and process to be executed, it is inherent that specific bits of the tcode field of Kobayashi would be reserved to represent specific types of information conveyed by the tcode field. The packet of Chou is analogous to the request and response packets of Claim 7 and functions in an analogous matter.

In reference to Claims 8 and 15, Chou teaches the limitations as applied to Claim 5 above and further teaches that the data transfer of the packets uses the IEEE 1394

standard format, so the transaction identification information is inherently a transaction label in accordance with said standard (See Figures 2 and 3, and Column 6 Lines 49-56 of Chou). Chou does not teach a means which makes transaction identification information within a request packet include indication information which indicates processing to be performed after reception of a response packet from a responding node when the request packet which is used for starting a transaction is transmitted to the responding node. Gehman teaches that data can be obtained from a node by sending a read request packet, according to the IEEE 1394 Standard, which contains a tcode field. The node then responds by packetizing the data according to the 1394 Standard and sends it to the requesting node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the tcode field of a 1394 Standard packet can provide information about the process to be executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). The packet of Chou is analogous to the request and response packets of Claims 8 and 15 and functions in an analogous matter.

In reference to Claim 18, Chou teaches the limits as applied to Claim 5 above and teaches the device included as part of electronic equipment (See Figure 2 and Column 6 Lines 30-32 of Chou) which further includes a CPU for processing the data received through the data transfer control device (See Figure 2, Column 6 Lines 66-67, and Column 7 Lines 1-2 of Chou), a mass storage device for storing the data that has been subjected to processing (See Figure 2 and Column 6 Lines 61-64 of Chou), and a display for outputting the data that has been subjected to processing (See Figure 2, Column 7 Lines 3-17 of Chou). Chou does not teach a means which makes transaction

identification information within a request packet include indication information which indicates processing to be performed after reception of a response packet from a responding node when the request packet which is used for starting a transaction is transmitted to the responding node. Gehman teaches that data can be obtained from a node by sending a read request packet, according to the IEEE 1394 Standard, which contains a tcode field. The node then responds by packetizing the data according to the 1394 Standard and sends it to the requesting node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the tcode field of a 1394 Standard packet can provide information about the process to be executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). The packet of Chou is analogous to the request and response packets of Claim 18 and functions in an analogous matter.

In reference to Claim 21, Chou teaches the limits as applied to Claim 5 above and further teaches that the CPU can take in data to be subject to processing (See Figure 2). Since the internal bus is bidirectional (See Figure 2 and Column 6 Lines 47-48), and since the interface circuitry can both send and receive data (See Figure 2 and Column 6 Lines 49-60), it is inherent that the CPU can perform processing on data that is to be transferred to another node through the interface circuit and the bus. Chou further teaches that data to be subjected to processing can be taken in through a keyboard, a mouse, or the 1394 link (See Figure 2 and Column 7 Lines 3-10). Chou does not teach a means which makes transaction identification information within a request packet include indication information which indicates processing to be performed after reception of a response packet from a responding node when the

request packet which is used for starting a transaction is transmitted to the responding node. Gehman teaches that data can be obtained from a node by sending a read request packet, according to the IEEE 1394 Standard, which contains a tcode field. The node then responds by packetizing the data according to the 1394 Standard and sends it to the requesting node (See Column 5 Lines 30-55 of Gehman). Kobayashi teaches that the tcode field of a 1394 Standard packet can provide information about the process to be executed (See Figure 7 and Column 5 Lines 35-42 of Kobayashi). The packet of Chou is analogous to the request and response packets of Claim 21 and functions in an analogous matter.

One of ordinary skill in the art at the time the invention was made would combine the device of Chou with the packet communication formats of Gehman and Kobayashi, resulting in the inventions of Claims 4, 5, 6, 8, 15, 18, and 21, in order to provide a means for a device to access a bus management register across a 1394 link (See Column 5 Lines 30-33 of Gehman).

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou as applied to Claim 9 above, and further in view of Nishijima and Longwell et al. ("Longwell").

Chou teaches the limitations of Claim 10 as applied to Claim 9 above. Chou does not teach a first address storage means which stores a transmission area start address for reserving a transmission area in the second data area, a second address storage means which stores a transmission area end address for reserving a

transmission area in the second data area, a third address storage means which stores a reception area start address for reserving a reception area in the second data area, and a fourth address storage means which stores a reception area end address for reserving a reception area in the second data area.

Nishijima teaches a memory area that is divided into a transmission area and a reception area (See Abstract and Figures 5 and 6 of Nishijima). Longwell teaches a means of storing a first start address, a second start address, a first address range (analogous to the first end address of Claim 10), and a second address range (analogous to the second end address of Claim 10) (See Figure 16 and Column 14 Lines 17-28 of Longwell).

One of ordinary skill in the art at the time the invention was made would combine the device of Chou with the devices of Nishijima and Longwell, resulting in the invention of Claim 10, in order to keep the transmission and reception areas separate (See Figures 5 and 6 of Nishijima) and to provide the active or inactive status of those areas of memory (See Column 14 Lines 17-19 of Longwell).

Allowable Subject Matter

14. Claims 11, 12, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: Claims 11, 12, and 13 would be allowable over the prior art of record if rewritten in independent form because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts.

In reference to Claim 11, prior art fails to teach the transmission area start address and the reception area start address being set to the start address of the second data area, and the transmission area end address and the reception area end address being set to the end address of the second data area.

In reference to Claim 12, prior art fails to teach both the transmission area start address and the transmission area end address being set to either the start address or the end address of the second data area, the reception area start address being set to the start address of the second data area, and the reception area end address being set to the end address of the second data area.

In reference to Claim 13, prior art fails to teach both the reception area start address and the reception area end address being set to either the start address or the end address of the second data area, the transmission area start address being set to the start address of the second data area, and the transmission area end address being set to the end address of the second data area.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

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tjc